CLAIMS

1. A method for optimizing body bias connections in a CMOS circuit substrate using a deep n-well grid structure, said method comprising:

performing a layout for said deep n-well grid structure;

determining an isolation region, and a connection region for placing body biased n-wells;

prioritizing a plurality of PFETs for placement in said body biased n-wells; and

performing a circuit layout wherein the plurality of PFETs are placed in the CMOS circuit wherein a subset of said plurality of PFETs are placed in the body biased n-wells in accordance with said prioritizing.

2. The method of Claim 1, wherein said deep n-well grid structure comprises an aperture that is approximately square with a dimension of substantially 7 microns.

3. The method of Claim 1, wherein the layout of the deep n-well grid structure is performed independently from the circuit layout.

4. The method of Claim 1, wherein the prioritizing is performed on the basis of inclusion on a critical path.

5. The method of Claim 1, wherein the prioritizing is performed on the basis of power dissipation

6. The method of Claim 1, wherein the prioritizing is performed on the basis of the effects of leakage current anticipated by modeling of the plurality of PFETs.

7. The method of Claim 1, further comprising determining a buffer region for separating said connection region and said isolation region.

8. A method for optimizing body bias connections in a CMOS circuit substrate using a deep n-well grid structure, said method comprising:

performing a layout for said deep n-well grid structure;

determining an isolation region, and a connection region for placing body biased n-wells;

prioritizing a plurality of PFETs for placement in said body biased n-wells; and performing a circuit layout wherein the plurality of PFETs are placed in the body biased n-wells in accordance with said prioritizing of the PFETs.

9. The method of Claim 8, wherein said deep n-well grid structure comprises an aperture that is approximately square with a dimension of substantially 7 microns.

10. The method of Claim 8, wherein the grid layout is performed independently from the circuit layout.

11. The method of Claim 8, wherein the prioritizing is performed on the basis of inclusion on a critical path.

12. The method of Claim 8, wherein the prioritizing is performed on the basis of power dissipation.

13. The method of Claim 8, wherein the prioritizing is performed on the basis of the effects of leakage current anticipated by modeling of the PFETs.

14. A method for optimizing body bias connections in a CMOS circuit substrate using a deep n-well grid structure, said method comprising:

a) performing a circuit layout for said substrate;

b) prioritizing a plurality of PFETs for placement in a plurality of body biased n-wells;

c) selecting a set of dimensional parameters for said deep n-well grid structure from a set of available parameters;

d) selecting an alignment between said deep n-well grid structure and said circuit layout for a set of available alignments;

e) determining a score for said alignment;

f) repeating d) through e) until said set of available alignments is exhausted;

g) repeating c) through f) until said set of available parameters is exhausted; and

h) performing a layout for said deep n-well grid structure using the dimensional parameters and alignment having a score which exceeds a predetermined threshold.

15. The method of Claim 14, wherein the circuit layout is performed independently from the grid layout.

16. The method of Claim 14, wherein the prioritizing is performed on the basis of inclusion on a critical path.

17. The method of Claim 14, wherein the prioritizing is performed on the basis of a power dissipation

18. The method of Claim 14, wherein the prioritizing is performed on the basis of the effects of leakage current anticipated by modeling of the PFETs.

19. The method of Claim 14, wherein said layout comprises placing a subset of said plurality of PFETs in said body biased n-wells according to said prioritizing.

20. An integrated circuit comprising:

a deep n-well grid structure for providing body bias to connected transistors;

a first set of transistors coupled to said deep n-well grid structure and body biased; and

a second set of transistors isolated from said deep n-well grid structure and not body biased therefrom.

21. An integrated circuit as described in Claim 20, wherein said transistors are PFETs.

22. An integrated circuit as described in Claim 20, wherein said first set of transistors comprises transistors that are in a critical path of said integrated circuit.

23. A method for designing an integrated circuit device, said method comprising:

a) accessing a design of an integrated circuit device, said design comprising a plurality of transistors;

b) determining a first plurality of transistors that are connectable to a deep n-well grid within said design;

c) identifying a second plurality of transistors that are not to be connected to said deep n-well grid as a result of a determination; and

d) within said design, connecting said first plurality of transistors to said grid wherein said second plurality of transistors are not connected to said grid.

24. A method as described in Claim 23 wherein said determination of c) is based on design rule violations of said second plurality of transistors.

25. A method as described in Claim 23 wherein said determination of c) is based on circuit performance reasons.

26. A method as described in Claim 23 wherein said determination of c) is based on electrical constraints.

27. A method as described in Claim 23 wherein said determination of c) is based on resistivity.

28. A method as described in Claim 23 wherein said determination of c) is based on proximity of said grid to another circuit element.

29. A method as described in Claim 1 further comprising restricting said grid away from proximities of said second plurality of transistors.

30. A method for optimizing body bias connections in a CMOS circuit substrate using a deep n-well grid structure, said method comprising:

a) accessing a pre-existing circuit layout for said substrate;

b) prioritizing a plurality of PFETs for placement in a plurality of body biased n-wells;

c) selecting a set of dimensional parameters for said deep n-well grid structure from a set of available parameters;

d) selecting an alignment between said deep n-well grid structure and said circuit layout from a set of available alignments;

e) performing a layout for said deep n-well grid structure using the selected dimensional parameters and the selected alignment.

31. The method of Claim 30 further comprising

f) determining a score for said selected alignment;

g) repeating d) and f) until said set of available alignments is exhausted;

h) repeating c), d) and f) until said set of available parameters is exhausted, wherein said selected alignment results from said h).

32. The method of Claim 30, wherein the prioritizing is performed on the basis of inclusion on a critical path.

33. The method of Claim 30, wherein the prioritizing is performed on the basis of a power dissipation

34. The method of Claim 30, wherein the prioritizing is performed on the basis of the effects of leakage current anticipated by modeling of the PFETs.

35. The method of Claim 30, wherein said layout comprises placing a subset of said plurality of PFETs in said body biased n-wells according to said prioritizing.